B-2.

AND, NAND, OR, NOR logic Gates

objectives:

This experiment will examine the operation of the AND, NAND, OR, and NOR logic gates and compare the expected outputs to the truth tables for these devices.

READING:

MATERIALS NEEDED:

74 LS 04 1 EA

74 LS 32 1 EA

74 LS 08 1 EA

74 LS 00 1 EA

74 LS 02 1 EA

330Ω 1 EA

LED 1 EA

POWER SUPPLY

SUMMARY OF THEORY:

The NOT circuit or inverter performs the basic logic function of complementation. It may be identified by the presence of a bubble on the input or the output of the traditional logic symbol or a triangle on the IEEE/IEC logic symbol as seen in Figure 1. The inverter has one input and one output and the output is the complement of the input. Figure 1 contains the truth table for the NOT function.

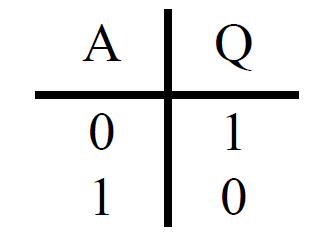
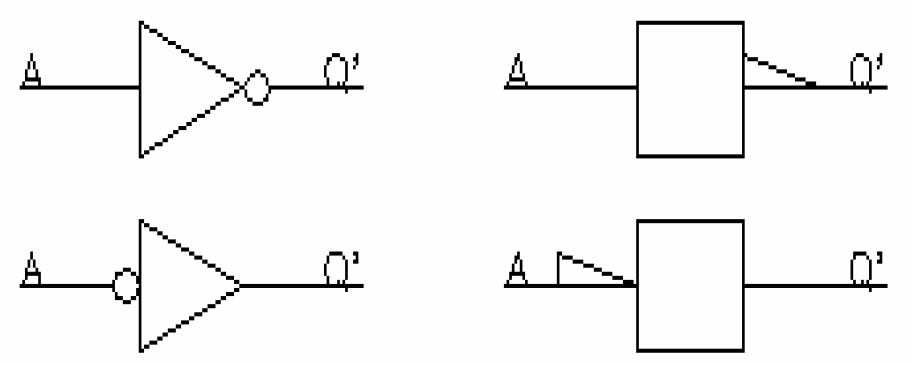


Figure 1 Logic Diagram

All logic gates have two or more inputs and one output. These logic gates accept digital logic levels on their inputs and will provide a digital logic level output which is dependent on the type of logic gate and the inputs applied to the gate. For the TTL logic family, any gate input that is not connected will be treated as if a logic 1 is present on that input. The number of different possible combinations of inputs is 2n where n is the number of inputs. Therefore, four unique combinations of inputs are possible for a two input gate.

The AND function is similar to the multiplication in mathematics, and provides a logic 1 output only when all the inputs of the gate are at logic 1, and logic 0 output for all other input combinations. Figure 2 contains the logic symbols and truth table for the AND function. The Boolean Equation for a 2 input AND gate, the Boolean Equation is:

(1)

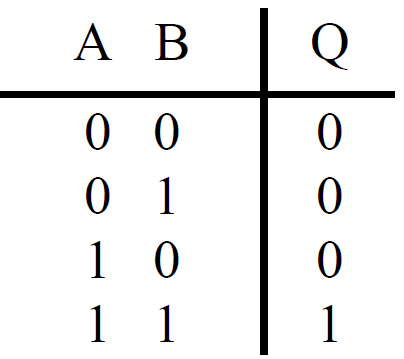
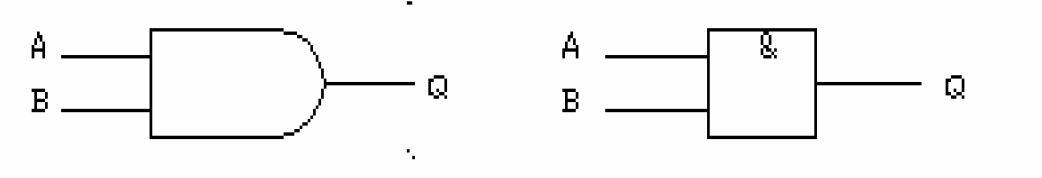


Figure 2 Logic Diagram

The NAND function is the complement of the AND function and the logic symbols have the inversion on the output. The NAND function provides a logic 0 on the output only when both inputs are logic 1, and a logic 1 output for all other combinations. The logic diagrams and the truth table are in Figure 3. The Boolean Equation for a NAND gate is:

(2)

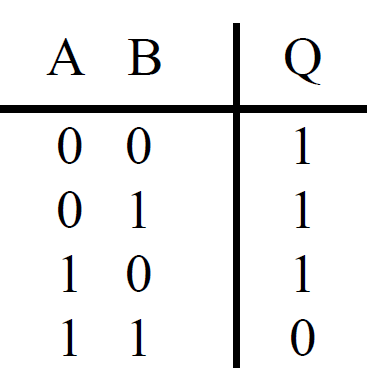


Figure 3 Logic Diagram

The OR function is similar to the mathematical function of addition and the output for the OR gate may be analyzed using the laws of addition. The logic operator for the OR function is a + sign. The output will be logic 0 only if all the inputs are logic 0, and the output will be logic 1 anytime any input is at logic 1. The logic symbols and the truth table for the OR gate may be found in Figure 4 and the Boolean Equation for this function is:

(3)

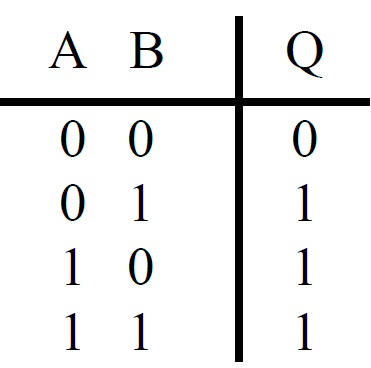
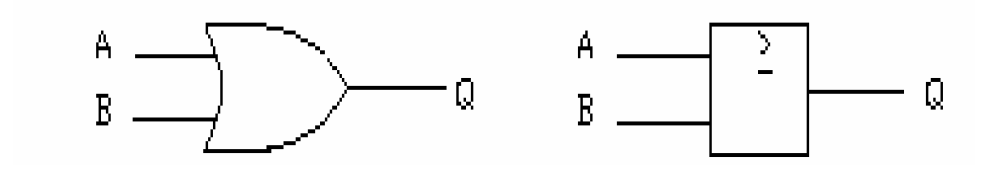


Figure 4 Logic Diagram

The complement of the OR function is the NOR function and the logic symbol has the inversion present on the output. Figure 5 contains the logic diagram and the truth table for the NOR function and the Boolean Equation is:

(3)

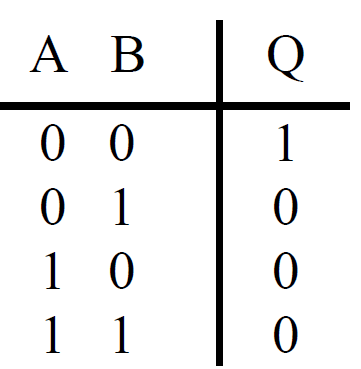


Figure 5 Logic Diagram

If we take all the inputs of a NAND gate or a NOR gate and connect them together, we will have an inverter or NOT function. This may be useful in logic design when an inverter is required. If we have a NAND gate that is not used for the circuit and we need an inverter, we can construct the inverter by connecting all the inputs together and connecting the gate in the normal manner. The connection of the NAND gate and the NOR gate as an inverter may be found in Figure 6.

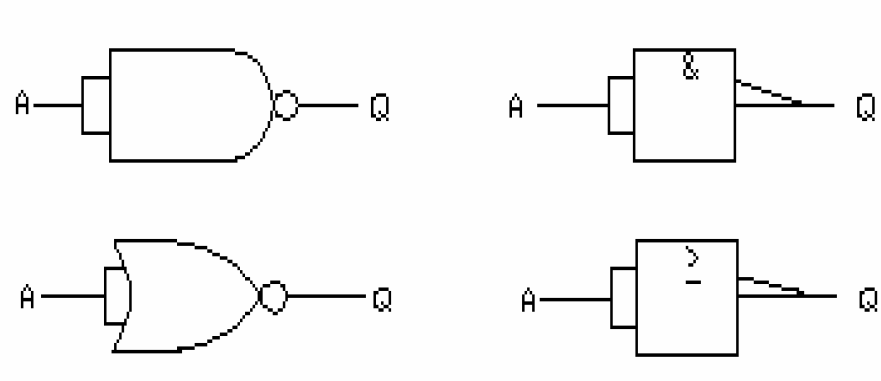


Figure 6 Logic Diagram

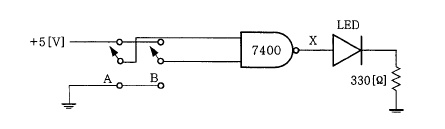


Figure 7 74XX Gates

Procedure

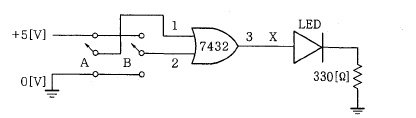
1. Draw the entire logic diagram with pin functions for the 74LS00, the 74LS02, the 74LS08, and the 74LS32. Label all pins and note their function.

1. Build the below circuit using 74LS00. Fill in below Table with the logic levels using LED lamp, and the output voltage as measured with the DVM(Digital Voltage Meter).



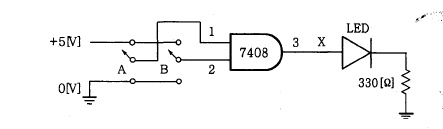
|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. Build the below circuit using the 74LS02. Fill in below Table with the logic levels using LED lamp, and the output voltage as measured with the DVM.



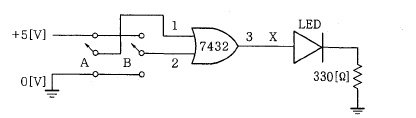
|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. Build the below circuit using the 74LS08. Fill in below Table with the logic levels using LED lamp, and the output voltage as measured with the DVM.



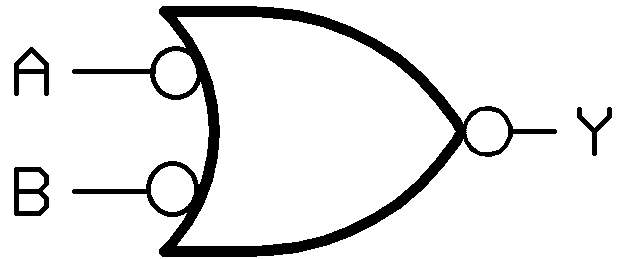
|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. Build the below circuit using the 74LS32. Fill in below Table with the logic levels using LED lamp, and the output voltage as measured with the DVM.



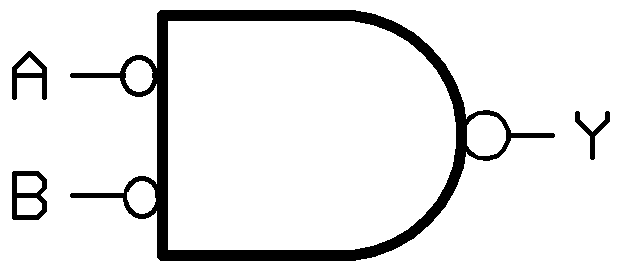
|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. Construct the below circuit using the 74LS02 with 74LS04. Fill in below Table with the logic levels and voltages.



|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. Construct the below circuit using the 74LS00 with 74LS04. Fill in below table with the logic levels and voltages.



|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **1** | **X** |  |  |

1. For procedure ②, leave another input of a 74LS00 unconnected and connect the other input to a logic level as indicated by the A input of below table. Fill in the table with the logic outputs observed.

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **X** | **0** |  |  |
| **X** | **1** |  |  |

1. For procedure ③, leave another input of a 74LS02 unconnected and connect the other input to a logic level as indicated by the A input of below table. Fill in the table with the logic outputs observed.

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **X** | **0** |  |  |
| **X** | **1** |  |  |

1. For procedure ④, leave another input of a 74LS08 unconnected and connect the other input to a logic level as indicated by the A input of below table. Fill in the table with the logic outputs observed.

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **X** | **0** |  |  |
| **X** | **1** |  |  |

1. Leave For procedure ⑤, leave another input of a 74LS32 unconnected and connect the other input to a logic level as indicated by the A input of below table. Fill in the table with the logic outputs observed.

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **Q** | **Voltage** |
| **0** | **X** |  |  |
| **1** | **X** |  |  |
| **X** | **0** |  |  |
| **X** | **1** |  |  |